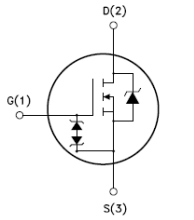
N-Channel Enhancement Mode Field Effect Transistor

BL10N65

FEATURES

- Extremely High dv/dt Capability.
- 100% AvalancheTtested.
- Gate Charge Minimized.
- Very Good Manufacturing Reliabilty.

Pb
Lead-free



TO-220AB

APPLICATIONS

- N-channel Enhancement mode Effect Transistor.
- Switching Applications.

MAXIMUM RATING operating temperature range applies unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate -Source Voltage	±30	V
I_D	Maximum Drain Current(continuous) at T_C=25℃ T_C=100℃	10 5.7	A
I_{DM}	Drain Current(pulsed)Note1	36	A
P_D	Power Dissipation at T_C=25℃	115	W
Vesd(G-S)	G-S ESD (HBM C=100pF,R=1.5kΩ)	4000	V
E_{AS}	Single Pulse Avalanche Energy (starting T_j=25℃,I_D=I_{AR},V_{DD}=50V)	300	mJ
dv/dt	Peak Diode Recovery Voltage Slope(Note2)	4.5	V/ns
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	62.5	℃/W
T_j T_{stg}	Operating Junction and StorageTem-perature Range	-55 to +150	℃

Note:1.Pulse width limited by safe operating area

2.I_{SO}≤12A,di/dt≤400A/us,V_{Peak}<$V_{(BR)DSS}$

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ELECTRICAL CHARACTERISTICS @ Ta=25℃ unless otherwise specified

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	600	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V V_{DS}=650V,V_{GS}=0V,T_C=125℃	-	-	1 50	μA
Gate-body Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±10	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	3	3.75	4.5	V
Static drain-Source On-resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=4.5A	-	0.65	0.75	Ω
Forward Transconductance	g_{fs}	V_{DS}=15V,I_D=4.5A	-	7.8	-	A
Forward on Voltage	V_{SD}	I_{SD}=12A,V_{GS}=0	-	-	1.5	V
Input Capacitance	C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz	-	1370	-	pF
Output Capacitance	C_{OSS}		-	156	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	37	-	pF
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 300V, I_D=4A, R_G= 4.7Ω,V_{GS}=10V	-	20	-	ns
Rise Time	t_R		-	20	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	55	-	ns
Fall Time	t_F		-	30	-	ns
Total Gate Charge	Q_g	V_{DS}=480V,V_{GS}=10V I_D=8A	-	50	70	nC
Gate-source Charge	Q_{gs}		-	10	-	nC
Gate-drain Charge	Q_{gd}		-	25	-	nC
Reverse Recovery Time	Trr	I_{SD}=8A,V_{DD}=40V dIF/dt=100A/μs,T_j=150℃	-	570	-	ns
Reverse Recovery Charge	Qrr		-	4.3	-	μC
Reverse Recovery Current	I_{RRM}		-	15	-	A

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TYPICAL CHARACTERISTICS @ Ta=25℃ unless otherwise specified

Figure 2. Safe operating area for TO-220 / I²PAK / D²PAK

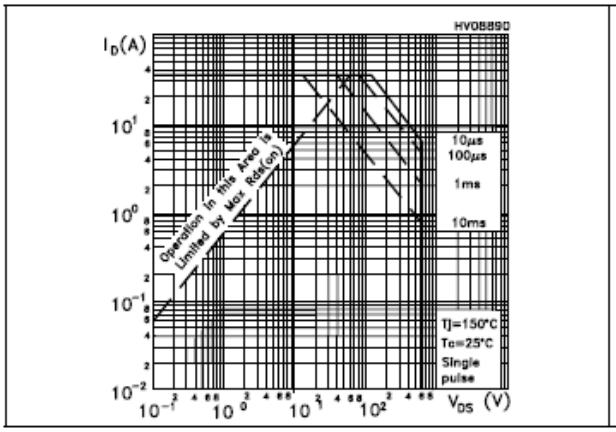

Figure 3. Thermal impedance for TO-220 / I²PAK / D²PAK

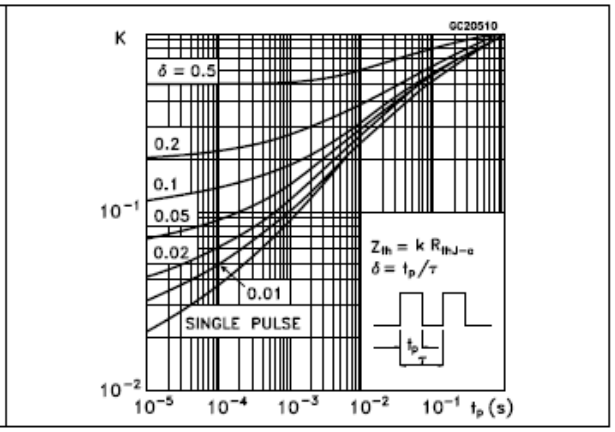

Figure 4. Safe operating area for TO-247

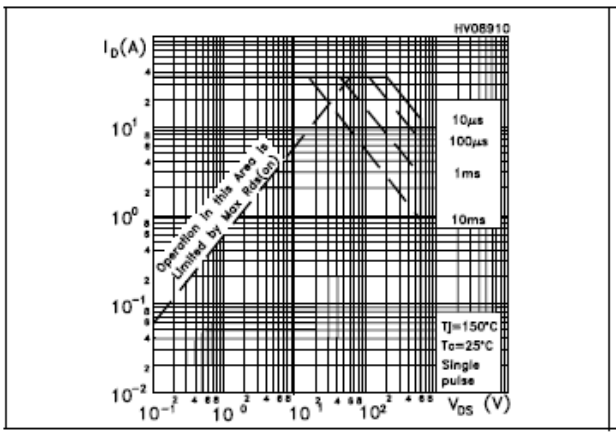

Figure 5. Thermal impedance for TO-247

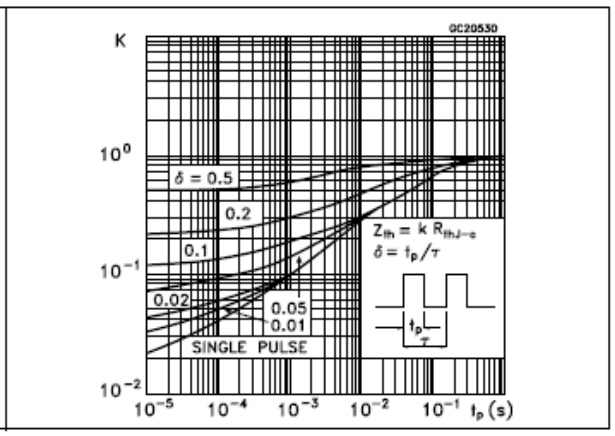

Figure 6. Safe operating area for TO-220FP

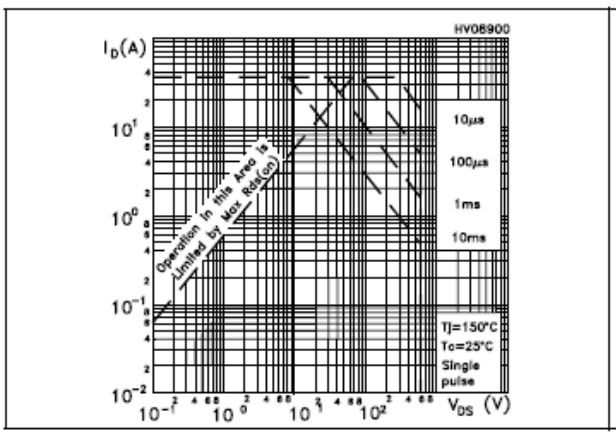

Figure 7. Thermal impedance for TO-220FP

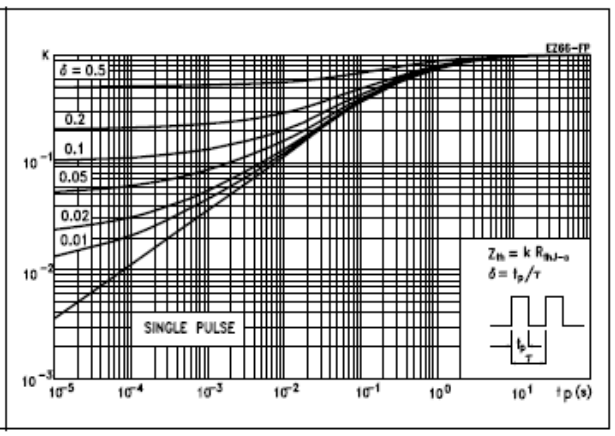

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Figure 8. Output characteristics

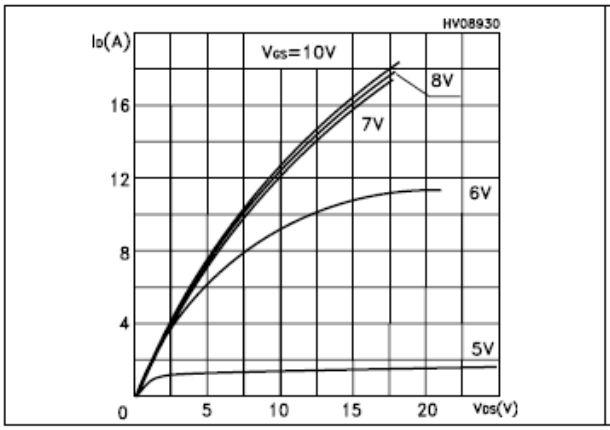

Figure 9. Transfer characteristics

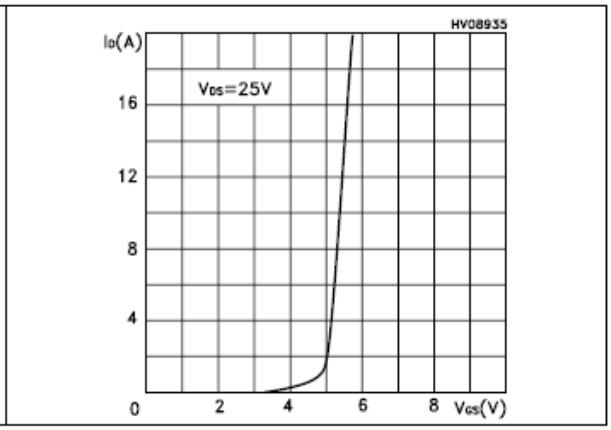

Figure 10. Transconductance

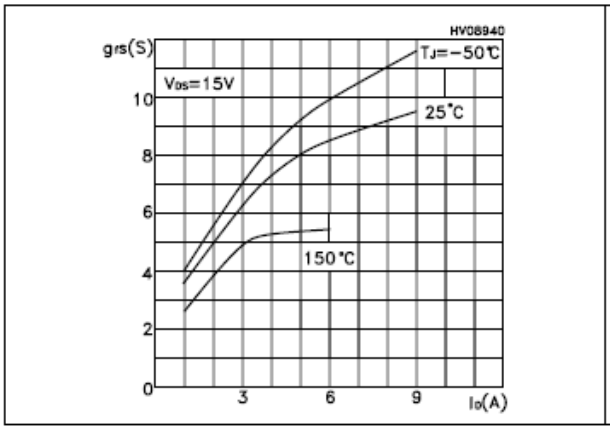

Figure 11. Static drain-source on resistance

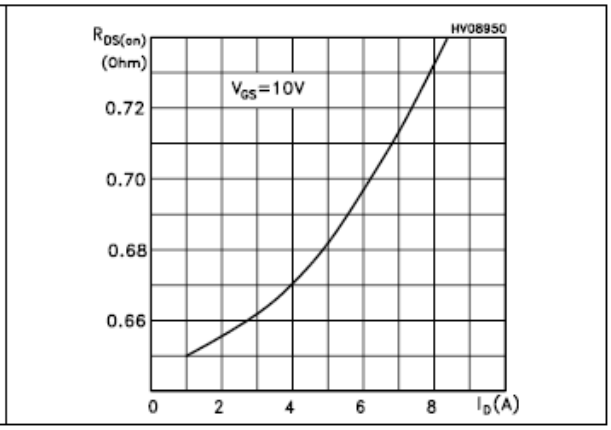

Figure 12. Gate charge vs gate-source voltage

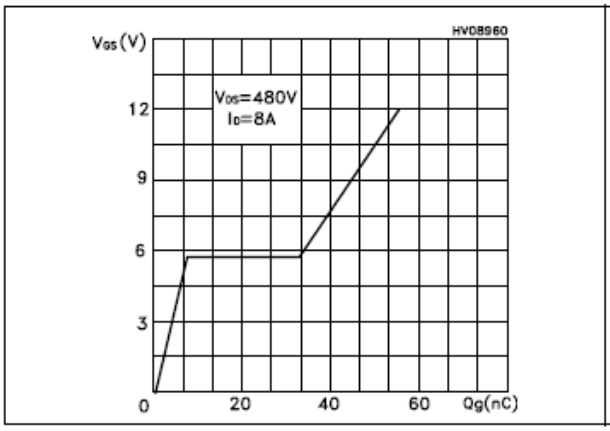

Figure 13. Capacitance variations

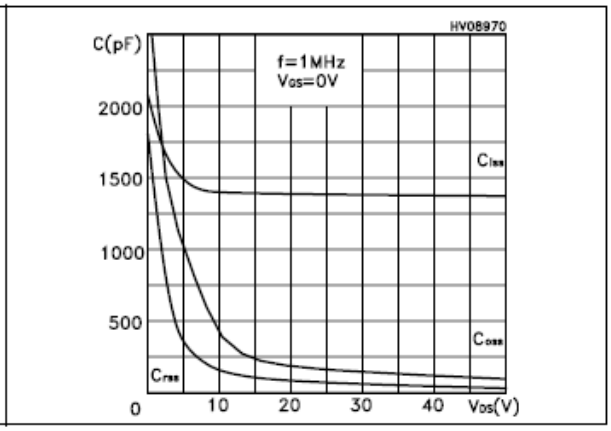

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Figure 14. Normalized gate threshold voltage vs temperature

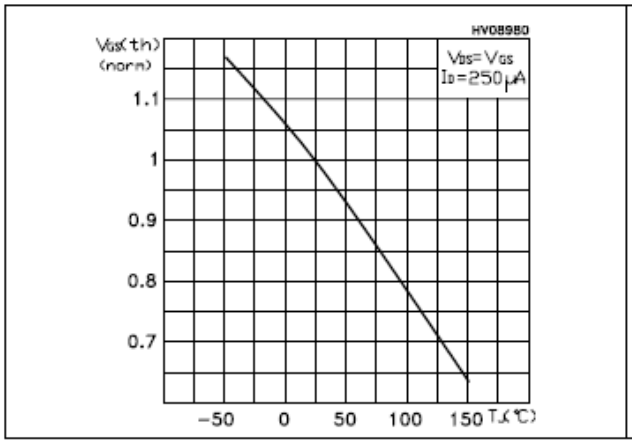


Figure 15. Normalized on resistance vs temperature

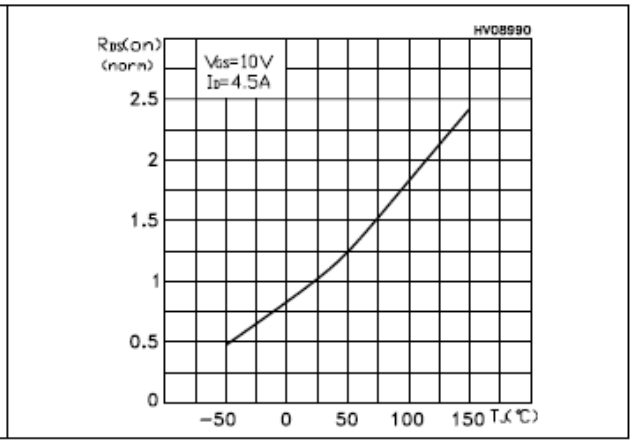


Figure 16. Source-drain diode forward characteristics

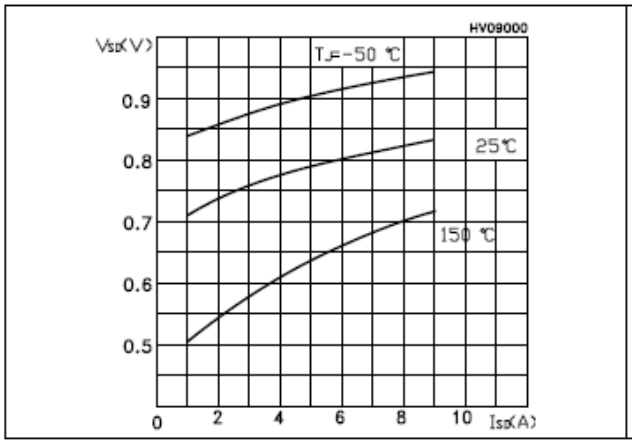


Figure 17. Maximum avalanche energy vs temperature

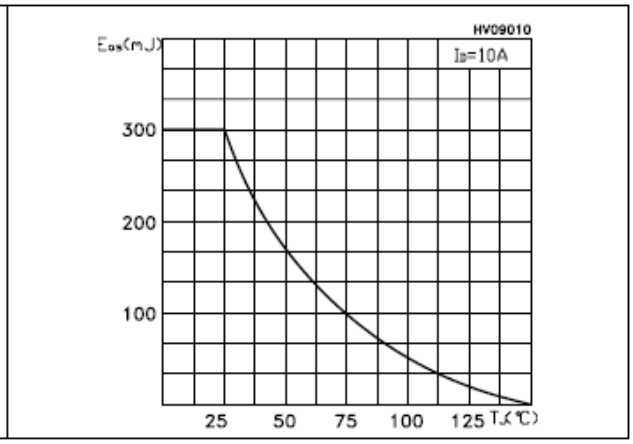
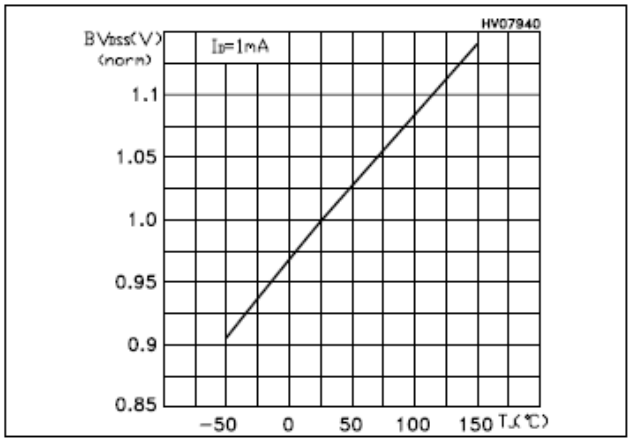


Figure 18. Normalized B_{VDSS} vs temperature



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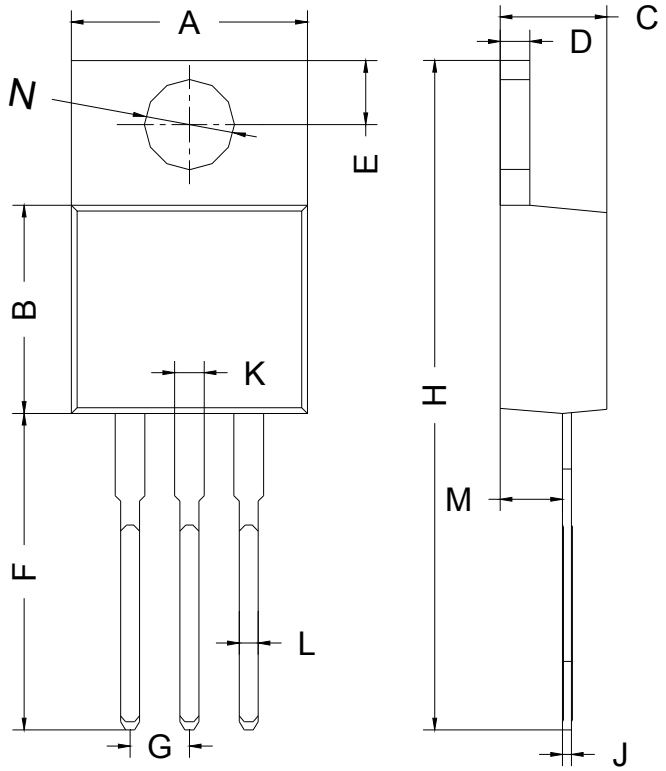
PACKAGE OUTLINE

Plastic surface mounted package TO-220AB



TO-220AB		
Dim	Min	Max
A	9.80	10.30
B	8.70	9.10
C	4.57 Typical	
D	1.27 Typical	
E	2.64	2.84
F	13.14	13.74
G	2.44	2.64
H	28.03	28.83
J	0.38 Typical	
K	1.22	1.32
L	0.71	0.91
M	2.50 Typical	
N	3.86 Typical	
All Dimensions in mm		